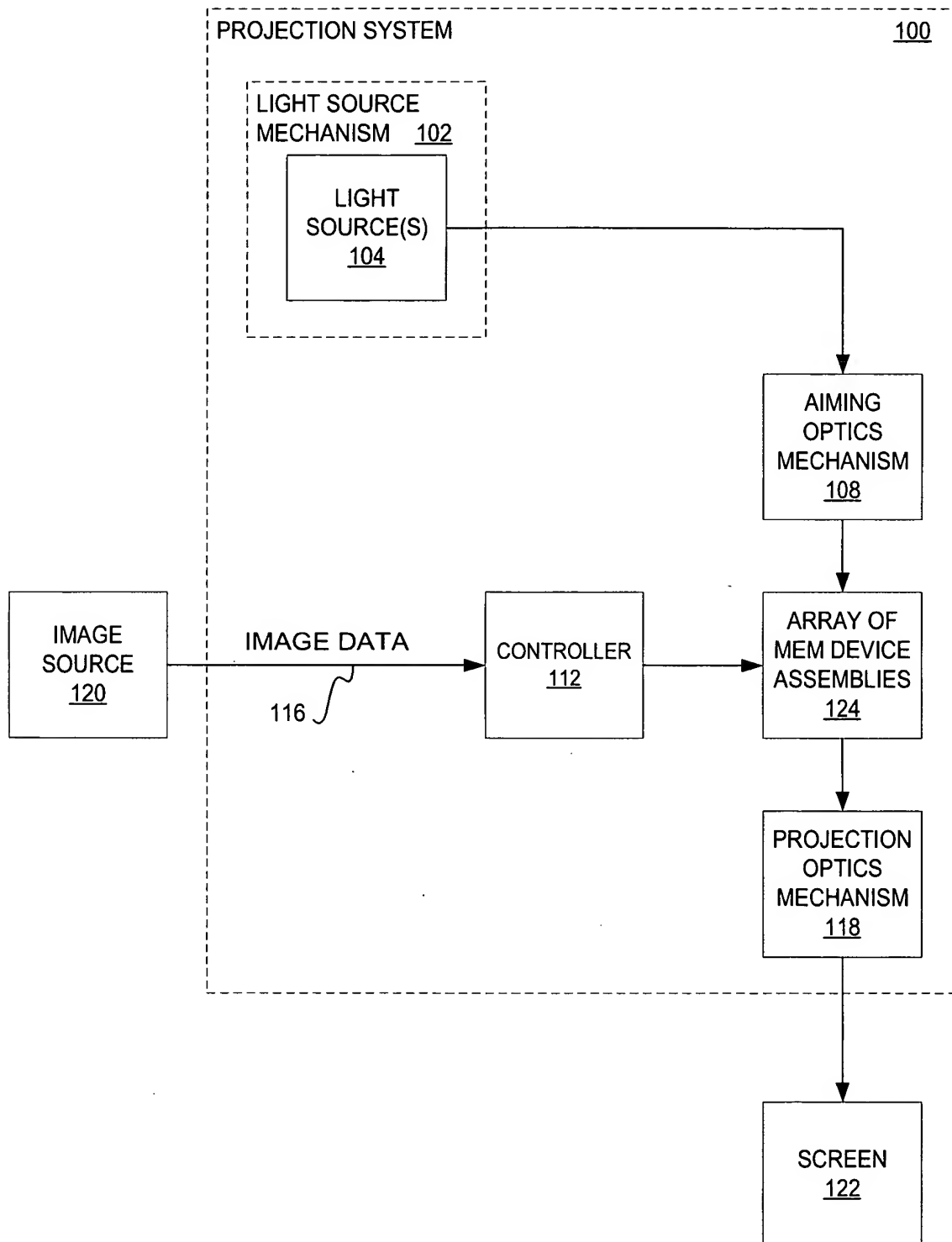


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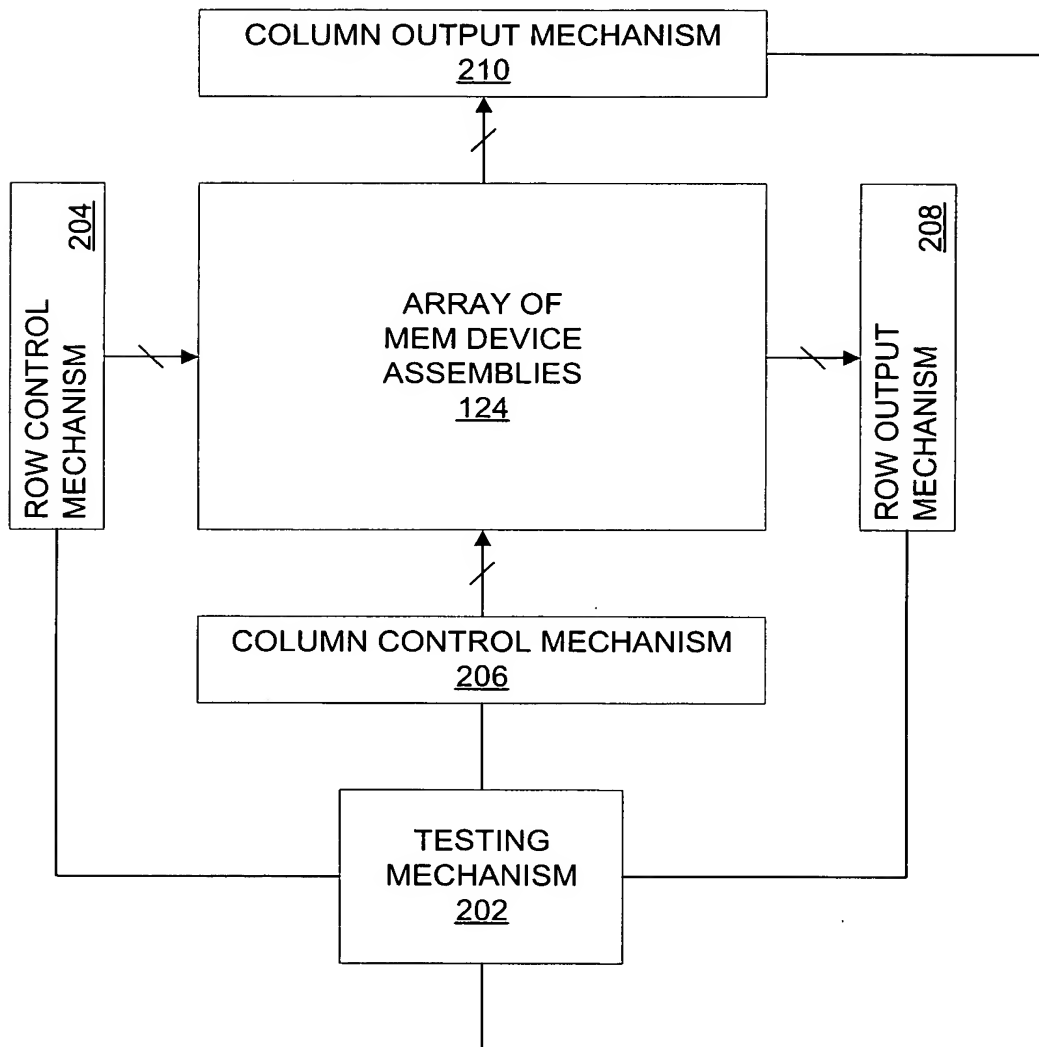
**FIG 1**



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FIG 2

100



**FIG 3**

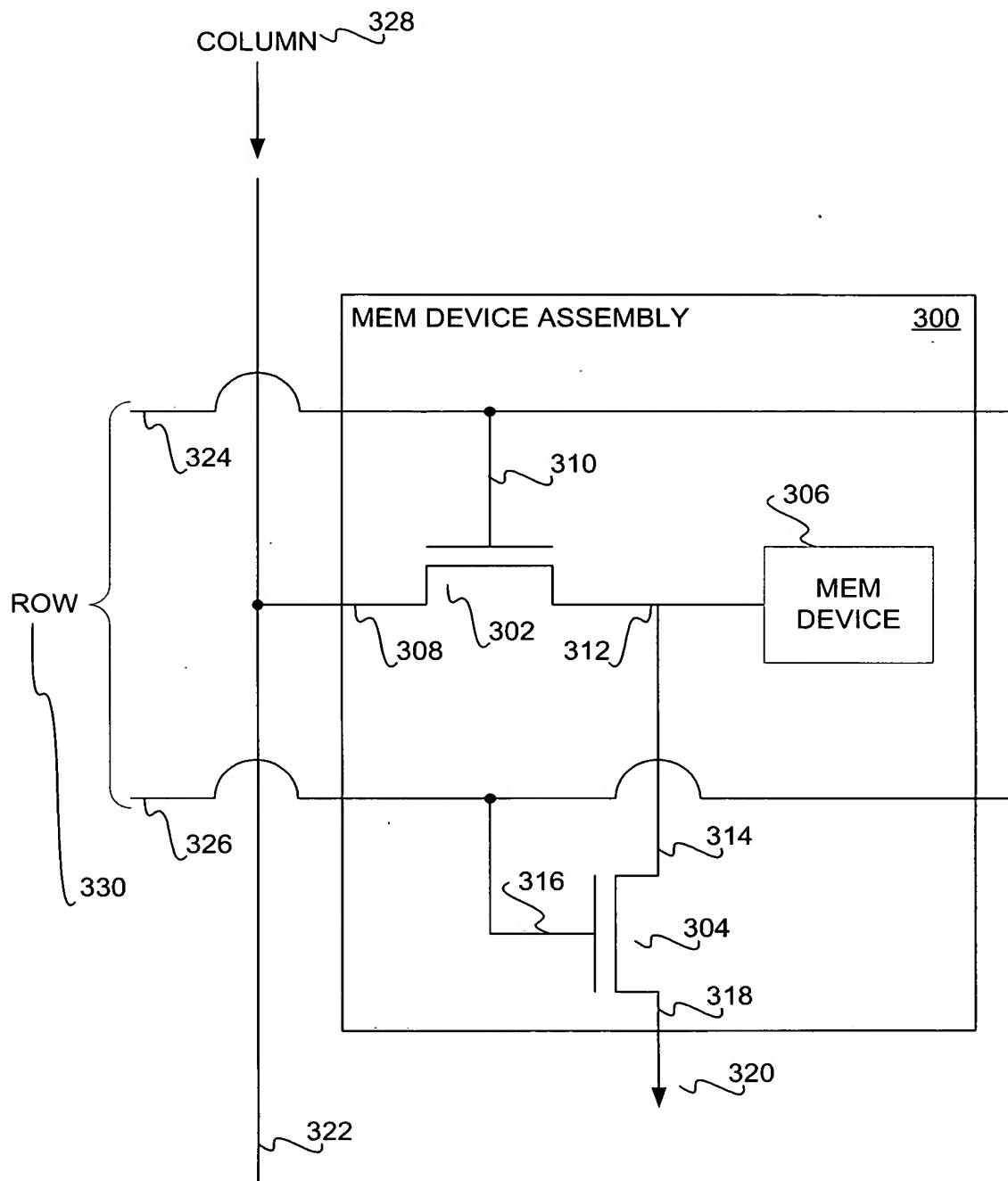


FIG 4

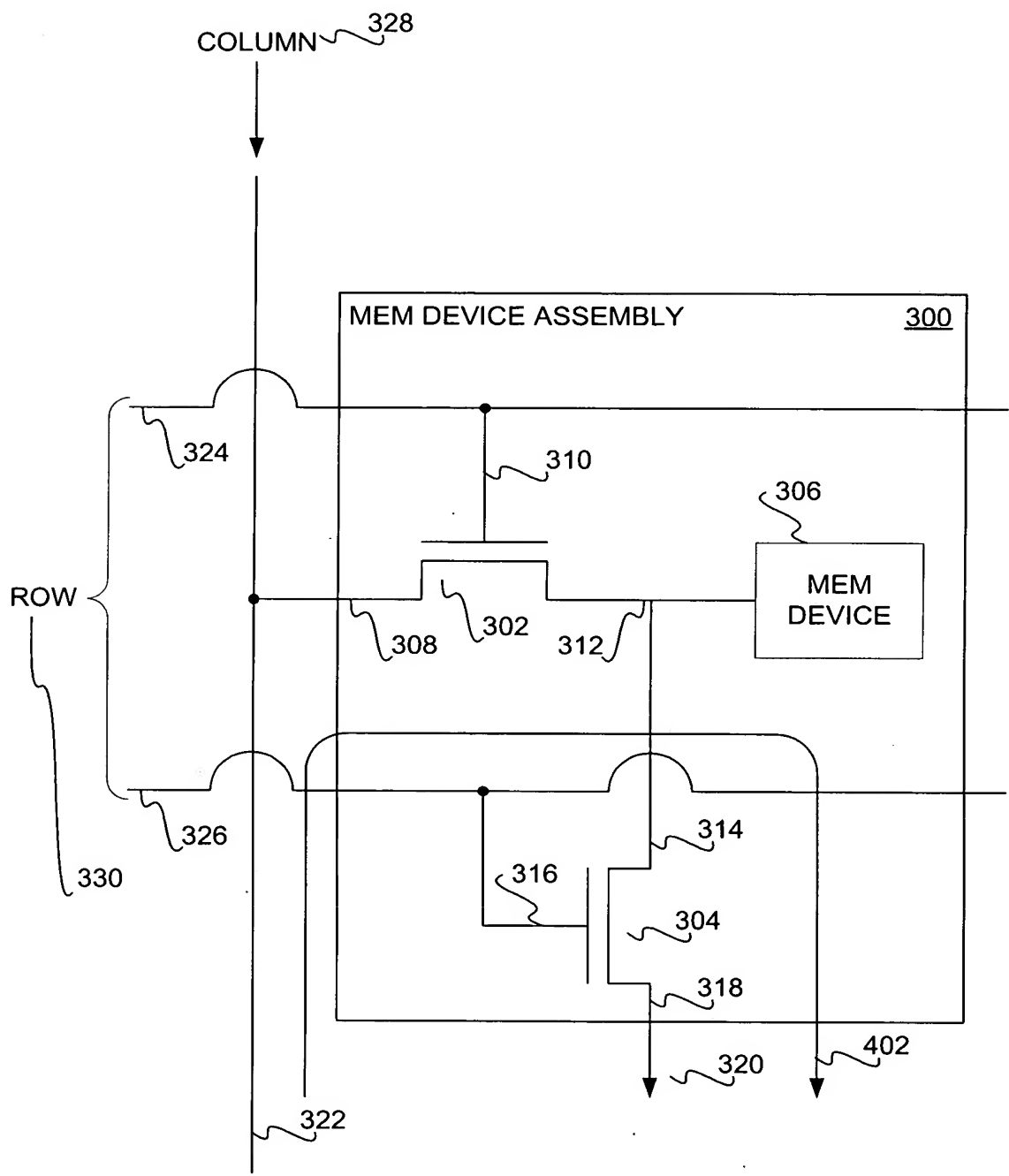
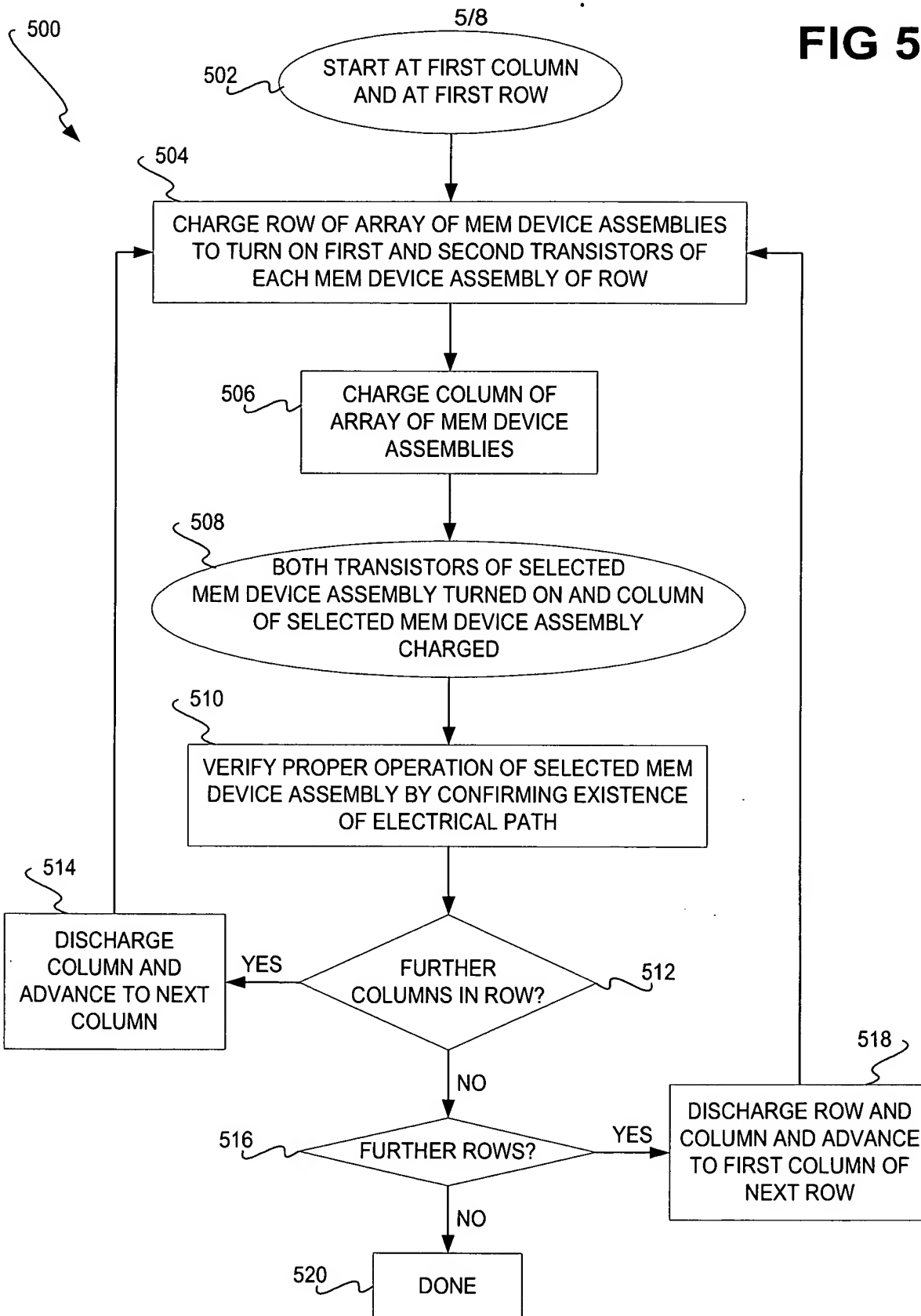


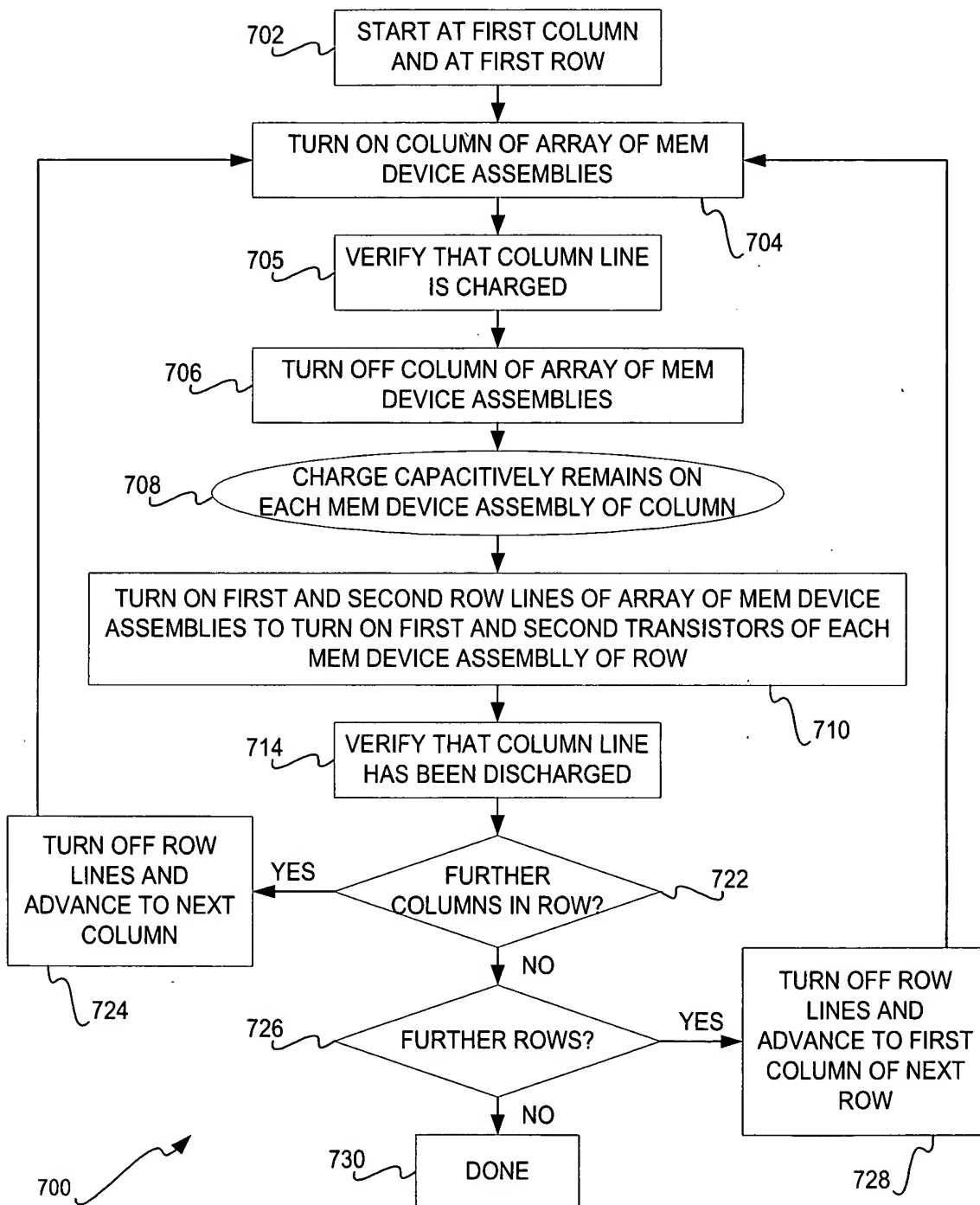
FIG 5



The diagram illustrates a memory device assembly 300. A vertical line represents the COLUMN line 328, and a horizontal line represents the ROW line 330. The assembly includes a MEM DEVICE ASSEMBLY 300. The circuit features a crossbar array with access transistors 302 and 304. The access transistors are controlled by row lines 324 and 326, and column lines 322 and 320. The memory device 306 is connected to the access transistors. The diagram also shows control signals 602, 604, 606, and 608, and states ON and OFF for the access transistors.

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FIG 7



**FIG 8**

